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Inventor(s): Munir H. Nayfeh, Joel Therrien, Gennadiy Belmoin

For: SILICON NANOPARTICLE FIELD EFFECT TRANSISTOR AND TRANSISTOR MEMORY DEVICE

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Enclosed are:

(X) 17 pages of specification, including 8 claims and an abstract.
( ) an executed oath or declaration, with power of attorney.
(X) an unexecuted oath or declaration, with power of attorney.
(X) 9 sheet(s) of informal drawing(s).
( ) ___ sheet(s) of formal drawings(s).
( ) Assignment(s) of the invention to _____.
( ) Assignment Form Cover Sheet.
( ) A check in the amount of $_____ to cover the fee for recording the assignment(s) is enclosed.
( ) Information Disclosure Statement.
( ) Form PTO-1449 and cited references.
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Fee Calculation For Claims As Filed

a) Basic Fee							$ 690.00
b) Independent Claims	3	- 3 =	0	x	$ 78.00	=	$ 0
c) Total Claims	8	- 20 =	0	x	$ 18.00	=	$ 0
d) Fee for Multiple Claims					$260.00	=	$
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Registration No. 35,132

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SILICON NANOPARTICLE FIELD EFFECT TRANSISTOR AND TRANSISTOR MEMORY DEVICE

FIELD OF THE INVENTION

The present invention concerns transistors. More particularly, the invention concerns single electron technology transistors, being transistors in which one-by-one transport of electrons controls device operation.

REFERENCE TO RELATED APPLICATION

This application is a continuation-in-part application of prior application to Nayfeh et al., Serial No. 09/426,204, entitled SILICON NANOPARTICLE STIMULATED EMISSION DEVICES, filed on October 25, 1999.

INCORPORATION BY REFERENCE OF COMMONLY OWNED RELATED APPLICATION

A co-pending and commonly owned application to Nayfeh et al., Serial No. 09/426,389, entitled SILICON NANOPARTICLES AND METHOD FOR PRODUCING THE SAME, filed on October 22, 1999, is incorporated by reference herein.

BACKGROUND OF THE INVENTION

Transistors are the basic building block of electronic devices. The power of a transistor depends, in large part, on its switching speed and its power requirements. Faster switching transistors offer improved performance. Transistors having lower power requirements offer energy conservation and reduced heating. The latter effects are especially important in devices which rely upon self contained power sources.

The power required to switch a transistor is a function of the amount of current necessary to cause device operation. Much research has been conducted in an effort to reduce the amount of current. The end goal is a device in which operation is caused by a single electron. In single electronics (single electron technology), device operation is based on the concept of one carrier for one bit of information. That is, it is based on one-by-one manipulation of electrons through a small sub-structure, and specifically a transistor.

American researchers first made a transistor that relies on a single electron about fifteen years ago, employing techniques used to make advanced semiconductor chips. They also built a single electron device in which a semiconductor substrate is coated with a thin layer of an insulating material and sprayed minute blobs of indium onto it. They then positioned the tip of a scanning tunneling microscope over it. By manipulating the voltages applied to the tip and the substrate, the researchers controlled the movement of single electrons in and out of the blob. A challenging problem for room temperature operation of such devices is that of thermal fluctuations.

So far, reasonably long range quantum effects on transport properties have been mostly observed near liquid helium / liquid nitrogen temperatures. An important step in the practical development of the single electron devices is therefore the ability to produce operation at higher temperatures, e.g., room temperatures. Thus, there is a need for an improved device in which operation of the device is controlled by the flow of an electron. It is an object of the invention to provide such an improved device, in the form of a silicon

nanoparticle field effect transistor.

SUMMARY OF THE INVENTION

The present invention concerns a transistor including silicon nanoparticles. Silicon nanoparticles are a previously unknown material. The silicon nanoparticles and a method for making the same are described in co-pending application Serial No. 09/426,204, to Nayfeh et al. entitled SILICON NANOPARTICLE STIMULATED EMISSION DEVICES, which is incorporated by reference herein.

In a preferred embodiment, the silicon nanoparticles occupy a gate region of the transistor. The resulting transistor is a transistor in which single electron flow controls operation of the transistor. Room temperature operation is possible with the novel transistor structure by radiation assistance, with radiation being directed toward the silicon nanoparticles to create necessary holes in the quantum structure for the flow of an electron.

The transistor of the invention also forms the basis for a memory device. The device is a flash memory device which will store electrical charge instead of magnetic effects.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features, objects, and advantages of the invention will be apparent by reference to the detailed description and the drawings, of which:

FIG. 1 depicts an experimental configuration where the tip of a scanning tunneling microscope is placed over a film material at a constant height to simulate a two terminal device;

FIG. 2 is the I-V response where the tunneling current was recorded while the voltage of the tip was varied with respect to the (grounded) substrate in the range -6 to +3 eV;

FIG. 3 gives the derivative of the I-V curve, shown in FIG. 2;

FIG. 4 is the I-V response of the experimental set up of FIG. 1, taken with the radiation from a mercury lamp;

FIG. 5 is the derivative of the I-V curve of FIG. 4;

FIG. 6 is an exemplary single electron silicon nanoparticle transistor of the invention;

FIG. 7 is an exemplary flash memory device of the invention, depicted in cross-section;

FIG. 8 illustrates a silicon nanoparticle gun; and

FIGS. 9a-9c depict operations of the FIG. 7 memory device.

DETAILED DESCRIPTION OF THE INVENTION

The present invention concerns single electron transistor devices which rely upon elemental silicon nanoparticles. The silicon nanoparticles provide a set of discrete levels for electron capture with energy spacing much larger than the thermal fluctuation energy.

Silicon nanoparticles of diameter ~ 1 nm, have a discrete set of states resulting from the quantum mechanical wave-like nature of electrons, capable of capturing/emitting single charge carriers, with an energy spacing on the order of 1 electron volt, and a discrete set of electric charging potential energy of 0.24 eV spacing. We demonstrated single electron transport through the particles at room temperature. The I-V spectra, taken using a scanning tunneling microscope, show single electron charging effects at a spacing of ~ 0.26 eV. In addition, upon light irradiation, and superimposed on the charging resonances, near one hundred percent resolved single electron conductance resonance are observed with a spacing consistent with the spacing of the energy levels of the quantum dots (the nanoparticles). This development permits single electron transistors that operate at room

temperatures with radiation-assistance.

The discrete set of states resulting from the quantum mechanical wave-like nature of electrons in the silicon nanoparticles is capable of capturing/ emission single charge carriers. The energy is multiples of the basic unit $E = h^2 / 3md^2$ where m is the mass of an electron, h is Planck's constant, and d is the diameter of the particle. For the particles of the invention, $d \sim 1$ nm, providing an energy spacing of 1 electron volt, five decades greater than room temperature thermal energy fluctuations (0.025 electron Volt). Only thermal fluctuations at temperatures approaching 12,000 C, more than twice the temperature on the surface of the sun, may interfere with the single electron processes in the particles. Thus, transistor devices utilizing the particles of the invention will maintain single electron processes comfortably at room temperature or any other temperature encountered under laboratory or real field conditions. Such transistor devices are truly high temperature single electronics devices.

The spacing of the energy states is a sensitive function of the diameter of the particle (quadratic dependence). For a particle of 6 nm diameter, the spacing drops to 0.027 of an electron volt. For this size, fluctuations at room temperature are equal to the energy of single electron processes. Thus, to ensure high quality operation at room temperature, sizes reasonably below 6 nm must be used. Even for 6 nm, the device must be cooled to liquid nitrogen temperature to exhibit reasonably resolved single electron processes. Thus, it is preferred that transistor devices of the invention use silicon nanoparticles having approximately 1 nm diameters.

In addition to energy discreteness provided by quantum mechanical dynamics, there is an energy discreteness due to charging potential energy. For small enough particles, the electric capacitance C will be very small such that the presence of a single electron during capture raises the electric potential, e^2/C, by an amount larger than the energy associated with the thermal fluctuations. In this case, single electron processes may be exhibited in

terms of discrete values of the electric potential energy. The unit e^2/C due to a single electron is called the Coulomb blockade.

Thus, in the concept of single electron devices there is an interplay between three energies: the quantum energy, the charging energy, and the thermal fluctuation energy. It is basically an interplay between size and temperature. The capacitance of a spherical particle $C = 2\pi\epsilon d$ is proportional to the diameter d of the particle (the charging energy is inversely proportional to the diameter), whereas the quantum energy is inversely proportional to the square of the diameter. The potential energy due to the discreteness of the charge is therefore more important for larger sizes. At intermediate sizes, the two become comparable. The quantum energy dominates, however, for the silicon nanoparticles used in the present transistor. The single electron devices become operational at a given temperature if at least one of the two of these discrete systems dominate the energy of thermal fluctuation. For the transistor of the invention, the characteristic charging unit is 0.24 eV, smaller than the quantum energy (1 eV). But both are much larger than thermal fluctuation energy for room temperature (0.025 eV). The discreetness, hence the single electron processes, are also maintained at elevated temperatures as high as 12,000C.

Operation of the present transistor requires assistance. The silicon nanoparticle of ~ 1nm diameter is essentially non conducting because all of the electronic energy levels are filled with stationary electrons. Standard doping levels of 10^{15} / cm^3 boron atoms allocates only 10^{-6} electron vacancies per particle (essentially none). Even strong doping at a level of $10^{17}/cm^3$ would be insufficient. The lack of non conductivity, however, will not hamper the operation of the high temperature device based on the single electron charging effects. Moreover, the present invention provides means to create vacancies for electrons to be captured by the quantum energy levels, rendering single electronics operational at high temperatures via both the discreteness of energy and the single electron charging. Irradiation of the silicon nanoparticles creates the necessary vacancies for single electron

operation. Such operation has been experimentally demonstrated.

An experimental device, as shown in FIG. 1, was used to test the principles of the present invention. The experimental device of FIG. 1 models the action of a FET transistor using a scanning tunneling microscope 10. FIG. 1 depicts the experimental configuration where a tip 12 of the scanning tunneling microscope 10 is placed over a silicon nanoparticle film material 14 on a substrate 16 at a constant height. Silicon nanoparticles 18 contained in the film 14 are represented with an exaggerated dimension by the particle 18 in FIG. 1. In this two-terminal arrangement, the tip 12 acts as the source, while the substrate 16 acts as the drain. We probed the conductance of the particles by recording the I-V spectra of the film 14.

The FIG. 1 configuration may be represented by a double barrier model. The particles 18 represent the quantum well, with a vacuum barrier due to a gap between the particle and the tip 12, and a barrier due to a gap between the particles 18 and the substrate 16. In the experimental measurements, the tunneling current was set at 1 nA and the biasing voltage at 3V in a constant current mode, giving a tip height of several angstroms. The feedback loop was then disengaged allowing the tip 12 to be held in a constant height mode while taking the I-V spectra. While the voltage of the tip was varied with respect to the (grounded) substrate 16 from -6 to + 3 volts, the tunneling current was recorded.

The measurement results are given in FIGS. 2-5. FIG 2 is the I-V response where the tunneling current was recorded while the voltage of the tip was varied with respect to the (grounded) substrate in the range -6 to +3 eV with no light stimulus. The staircase due to charging is discernable, but not easily resolved. FIG. 2 gives an average of sixteen individual spectra. Averages over a larger number tend to exhibit drifts due to difficulty in maintaining a constant tip height, which may wash out the structure. FIG. 3, the derivative of the FIG. 2 I-V curve, clearly shows a progression of resonances at a spacing of 0.26 eV for both positive and negative tip biasing with respect to the substrate.

For the ultra-small silicon nanoparticles, the spacing of the energy levels, according to a standard theory of particle in a box is $E = h^2/3md^2$ which gives for d = 1.1 nm, and m = the mass of an electron, an energy spacing of Δ = 1.03 eV. Also, the capacitance of the particles is $C = 2\pi \epsilon d$, where ϵ is the permittivity of silicon which gives for d = 1 nm, and $\epsilon = 12\ \epsilon_0$ a capacitance of 6.7×10^{-19} F. The characteristic charging due to a single electron of charge e is $\delta = e^2/C = 0.24$ eV. According to theory, if the temperature is such that $kT << \delta, \Delta$, as is the case in the present experiment, effects due to the discreteness of the charge (charging effect) and the discreteness of the energy spectrum (level spacing) should coexist at room or higher temperature. Because $\Delta \geq \delta$, then the Δ series should appear as a modulation of the smaller period δ. However, we do not see any modulation at or close to Δ, and note that the measured spacing of the steps, 0.26 eV, is consistent with the characteristic single electronic charging, hence we interpret the observed resonance structure as due to charging. Thus, the single electron device is operational based on the charging effect.

To investigate the effect of light stimulation, data was also taken with the FIG. 1 experimental set-up, with the film 14 containing nanoparticles 18 being stimulated by the light from a mercury lamp. The radiation spectral width spans the range 300 nm to 600 nm with a maximum at 350. A Pyrex glass port through which the mercury stimulation light is coupled to the vacuum system has a transmittance cutoff at 270 nm. The I-V response, shown in FIG. 4, now shows quite visibly a second regular step structure superimposed on the spectrum taken under darkness conditions with no light stimulus as in FIGS. 2 and 3. The derivative of the FIG. 4 I-V curve, shown in FIG. 5, clearly shows the progression of the resonances at large negative biasing up to a tip biasing of -1 eV with respect to the substrate, with a period of 1.0 eV, equal to the particle's quantum level spacing.

In the biasing region where both series coexist ($\leq$ -1 Volt), current steps at dc voltage level obey a very simple rule: $e\eta\ (V_{n,k} - V_t) = \delta n + \epsilon_k$ with n = 0, 1, 2, ... is the

number of electrons already residing on the dot, k = 1,2, ... designate the energy level of the dot, η is the fraction of the capacitance of the collector from the total, ϵ_k is the energy of the kth level of the particle. The derivation of the simple expression applies for an initially empty particle, $kT \ll \delta, \Delta$, and $E > \epsilon_f$. The step appears when the voltage aligns the Fermi level of the emitter with the kth energy level of the particle, with an account of the dot charging by n electrons already residing there. This condition gives, for $\Delta \gg \delta$, a constant modulation period dominated by Δ. Thus, we relate the additional modulation resonances observed to the opening of tunneling channels as the Fermi energy level of the tip is scanned across the particle's energy levels.

The light effect may simply be understood in terms of hole generation. Under standard doping levels of $\sim 10^{15}$ / cm^3 boron atoms, as is typical for a wafer like that used to produce nanoparticles for experiments described herein, particles of 1 nm across contain less than one in a million holes, hence there are no empty levels for the injected electrons. Practical laboratory temperature would not be sufficiently high to induce holes. Light irradiation, however, creates the necessary holes for the process to proceed.

The present observations have some interesting implications for the relative tunneling rates in and out of the silicon nanoparticles. Since the charge accumulation is observed, then Γ^e the tunneling rate from the tip into the particles, must not be much smaller than Γ^c, the tunneling rate from the particle to the substrate. If $\Gamma^e \ll \Gamma^c$ the charge is not accumulated in the particles and the only visible structure is the one related to energy quantization. Moreover, according to theory, if the energy discreteness Δ is dominant as in this case, and $\Gamma^e / \Gamma^c \leq 1$, the two fine structures also can be easily separated: the energy quantization structure with larger period modulates the charging related superfine structure with smaller period. For $\Gamma^e / \Gamma^c \geq 1$, the modulation period is increased due to charge accumulation, and equals $\Delta + 2\delta$. Since the period measured for the discreteness of energy is equal to the atomic transitions, then it is concluded that Γ^e and Γ^c are comparable.

The data demonstrates the potential to operate radiation-assisted single electron transistors based upon the silicon nanoparticles, such as the transistor shown in FIG. 6. FIG 6 gives a schematic of the field effect transistor with the nanoparticles implanted in the gate oxide as a buried gate. It shows the source, drain, and gate electrodes 17a, 17b and 17c, with electric leads for voltage biasing, and it shows the nanoparticle floating buried gate (shown outside the gate area for purposes of illustration). The buried nanoparticle gate 18a is connected to a voltage source, thus it can be biased independent from the source-drain-external gate, or it can be used as floating gate with no biasing. The source-drain conductance may be directly derived from the I-V characteristic measured using a precision semiconductor parameter analyzer. The characteristic are measured while the source is grounded and the drain voltage fixed at 1 mV. The source-drain conductance oscillates when the gate voltage is varied if the particle size is such that single electron charging or the quantum energy spacing dominates thermal energies. The oscillation period is the single electron charging or quantum energy spacing. In the device of FIG. 6, silicon nanoparticles 18 are implanted in the gate area 20 of a Si MOSFET as a buried gate layer. Lateral transport across the source-drain channel of the transistor, through the particles, would exhibit single electron effects as a function of the gate biasing. UV irradiation can be used to switch the single electron operation. This device may act as a dual electrical and optical device. The nanoparticles may be photo or electro stimulated to produce blue laser beams within the body of the transistor. At the same time, it will operate as a single electronics device. In addition, if tunneling from the particle gate to the substrate or drain is slowed down by providing sufficient insulators such that $\Gamma^c << \Gamma^e$, then the transistor will act as a memory device.

Silicon particle floating flash memory devices operate on the use of media that store electric charge instead of using media that store magnetic effects. This requires electrical isolation of the sub elements of the media from each other and from the connection to the powering elements (source-drain). Silicon islands (particles or so called quantum dots)

which are electrically floating (electrically insulated from every other element) within the volume of the insulating oxide of the gate of a field effect transistor are the backbone of this device, shown in FIG. 7. FIG. 7 is a schematic cross section of a nanoparticle memory device, showing the source 30, drain 32, and the gate 34 of the device. The silicon nanoparticles 18 are sandwiched between a thin oxide 36 of 1-2 nm thickness (tunneling oxide) that has been grown on the channel face, and a somewhat thicker control oxide (~ 5 to 10 nm) grown over the particles. The device of FIG. 7 offers fast-access, low-power dissipation, and possible extreme down-scaling. As the race to extreme down-scaling of device size continues to achieve faster and more efficient devices, and dense packing, it is important to develop methods for synthesis of small enough silicon floating gates (particles) to be accommodated within the gate oxide. The fabrication technology must keep up with the down-scaling, such that it will become possible for the floating gates in flash memory to be reduced to the nanometer scale, effectively behaving like quantum dots. If so, then it will be fabricated with a minimum perturbation of conventional silicon technology, and operate at room or higher temperature. The ultra-small size of the nanoparticles of the invention allows the realization of such technology.

The deposition (sandwiching) the particles in the gate oxide may be accomplished using a Si nanoparticle gun. The gun delivers the particles onto the gate area simultaneously with the deposited control oxide. The concept of the particle gun is similar to an ion beam gun used for ion implantation. The particle's energy, however, need not be as high since they are to be deposited and not implanted. In the particle gun, a colloid of the particles in a volatile liquid (such as acetone, or alcohol) is used. A jet or stream of the colloid is leaked into the system. A mechanism such as a plasma, or a radiation source is used to electrically charge the particles. The particles will then be accelerated to the required energy. A Mass filter is used for size selectivity and to reject any residual material from the solvent.

A particle gun may be constructed as shown in FIG. 8. The gun includes a Si nanoparticle inlet 38 to deliver the particles. The inlet 38, which may be an atomizer, utilizes a colloid of the Si nanoparticles in a volatile liquid (such as acetone, water, or alcohol). A jet or stream of the colloid is shot or leaked into the Si particle ion source 40 of the gun. Most of the volatile solvent droplets will evaporate leaving the Si particles in flight. In the ion source 40, the particles get charged in their flight. The produced particle ions are accelerated (propelled) into a focusing lens 42, powered by a feedthrough electrical connection 44, where they get focused, collimated and accelerated. The accelerated particles enter into a velocity filter 46 for mass (size) selection and rejection of nonsilicon species such as residual solvent material. The velocity filter 46 is powered through a feedthrough 47 (some feedthroughs, e.g., a feedthrough for the inlet 38 are not pictured in FIG. 8 for simplicity of illustration). Mass selection is important to ensure that there is no material from the solvent in the Si nanoparticle beam. A mass selectivity of ~ 2/1000 can be achieved. The particle energy at the exit of the velocity filter 46 is in the range 500 to 10 keV. Finally, the particle beam enters a decelerator 48 which is capable of lowering the energy of the particles, delivering mass (size) selected particles with energies less than 500 eV (as low as 1 eV), though the deceleration 48 may be omitted if exit velocity is not a concern. Vacuum in the gun of FIG. 8 is monitored and controlled through vacuum port 50.

The memory device of FIG. 7 may be built by such techniques using a N-channel or a p-channel Si material. In N-channel memory where the channel is rich in excess electrons, biasing the gate positive relative to the source (grounded), and to the drain (biased at ~ 0.1 Volt) attracts electrons from the channel to tunnel through the thin oxide and charge the silicon nanoparticles (write step), as shown in FIGS. 9a-9b. Reversal of the charge from the silicon nanoparticles back to the channel may be achieved by reversing the polarity of the gate bias (erase step), as shown in FIG 9c. If there is negligible lateral leakage between silicon nanoparticles and eventual dissipation in the source-drain, then long term

storage of charge is attained and the obtained memory is robust. The number of charges that may be accommodated on each silicon nanoparticle depends on the size of the silicon nanoparticle and on the biasing of the gate relative to the source-drain. Large gate voltages lead to an increase in the number of stored electrons. Smaller silicon nanoparticle sizes lead to a large single electron charging, thus limiting the number of electrons.

In p-channel memory where the channel is rich in holes, biasing the gate negative relative to the source and to the drain attracts holes from the channel to tunnel through the thin oxide and charges the particles in the writing step. Erasure is achieved by reversing polarity of the gate voltage.

The effective memory threshold voltage shift that retains the charge on the particles is given by the simple expression: $V_T = \frac{qnt_0}{\epsilon_0} + \frac{1}{2}\frac{qnd}{\epsilon_p}$, where n is the surface density of the nanoparticles, q is the electronic charge, t_0 is the thickness of the control oxide, d is the diameter of the nanoparticle, and ϵ_0 and ϵ_p are the permittivities of the oxide and the particle respectively. For a particle density of 10^{12} /cm^2, t_0 = 7 nm, and a particle diameter of 1 nm, a shift of ~ 0.35 eV per one electron per particle is achieved. This shift is an excellent shift since it provides a change of five orders of magnitude in the subthreshold current of a transistor.

The ultra-small particles of the invention provide several advantages to transistor technology. First, they can be accommodated in extremely down-scaled transistors. Second, our preparation and colloid filtering, along with the mass analysis provided by the particle gun delivery system provide a high quality control on the definition and selection of the size. A narrow mass distribution (<0.25%) ensures that the discrete energy system is well defined and that the device threshold is sharp. Large variations in the size of an ensemble of particles turns the discrete spectrum into a quasi continuum and washes the device threshold. Previously, sizes smaller than 5 nm have not been achieved, and the size fluctuation exceeds 5 to 10 percent. Third, the particles are very small such that

the single electron charging and the quantum energy spacing is larger than the thermal energy, thus single electron processes are in operation at room or higher temperature. Moreover, since the discrete levels are spaced out considerably, then more than one level of the particle may be utilized, namely, the particles may be operated as a multi-level memory system. Fourth, the single electron characteristic charging energy is high enough such that it limits the number of electrons that can be accommodated on each particle to one. Fifth, the use of ultra-small particles allows us to attain a larger inner particle oxide thickness for the same particle density. Thicker oxide improves the isolation of particles, hence it limits the lateral leakage further, thus improving the memory of the device. Moreover, since a thin tunneling oxide is used, the nanoparticle memory can be operated at low voltages compared to conventional flash memory. The use of a thin oxide between the particles and the silicon channel allows charging via quantum tunneling instead of hot carrier injection at higher voltages. Direct tunneling is therefore desired in the charging and discharging of the Si particles to prevent hot-carrier degradation. Finally, lower voltages mean less electrons are accommodated on particles.

While various embodiments of the present invention have been shown and described, it should be understood that other modifications, substitutions and alternatives are apparent to one of ordinary skill in the art. Such modifications, substitutions and alternatives can be made without departing from the spirit and scope of the invention, which should be determined from the appended claims.

Various features of the invention are set forth in the appended claims.

WHAT IS CLAIMED IS:

1. A single electron transistor device comprising:

a source;

a drain;

a gate having a gate area; and

silicon nanoparticles implanted in said gate area.

2. The single electron device according to claim 1, further comprising a buried gate contact to electrically stimulate said silicon nanoparticles separately from a contact to said gate.

3. The single electron device according to claim 1, wherein said silicon nanoparticles have a diameter of approximately 1 nm.

4. The single electron device according to claim 1, wherein said silicon nanoparticles exhibit an energy spacing of approximately 1 eV.

5. A method for operating a single electron device, which has a source, a drain, a gate having a gate area, and at least silicon nanoparticles implanted in the gate area, comprising the steps of:

creating at least one electron hole in the silicon nanoparticles to enable the silicon nanoparticles to conduct a single electron at room temperature across the source and the drain; and

applying a voltage across the drain and the source.

6. The method of operating the single electron device according to claim 4, wherein said step of creating an electron hole in said silicon nanoparticles is accomplished by irradiating said silicon nanoparticles.

7. The method of operating the single electron device according to claim 5, wherein said step of creating an electron hole uses light having a spectral width between 300nm and 600nm.

8. A transistor memory device comprising:

a source;

a drain; and

a gate, said gate having a gate area with silicon nanoparticles contained in a control oxide and separate from a tunnel oxide disposed between said source and drain.

SILICON NANOPARTICLE FIELD EFFECT TRANSISTOR AND TRANSISTOR MEMORY DEVICE

ABSTRACT

A silicon nanoparticle transistor and transistor memory device. The transistor of the invention has silicon nanoparticles, dimensioned on the order of 1nm, in a gate area of a field effect transistor. The resulting transistor is a transistor in which single electron flow controls operation of the transistor. Room temperature operation is possible with the novel transistor structure by radiation assistance, with radiation being directed toward the silicon nanoparticles to create necessary holes in the quantum structure for the flow of an electron. The transistor of the invention also forms the basis for a memory device. The device is a flash memory device which will store electrical charge instead of magnetic effects.

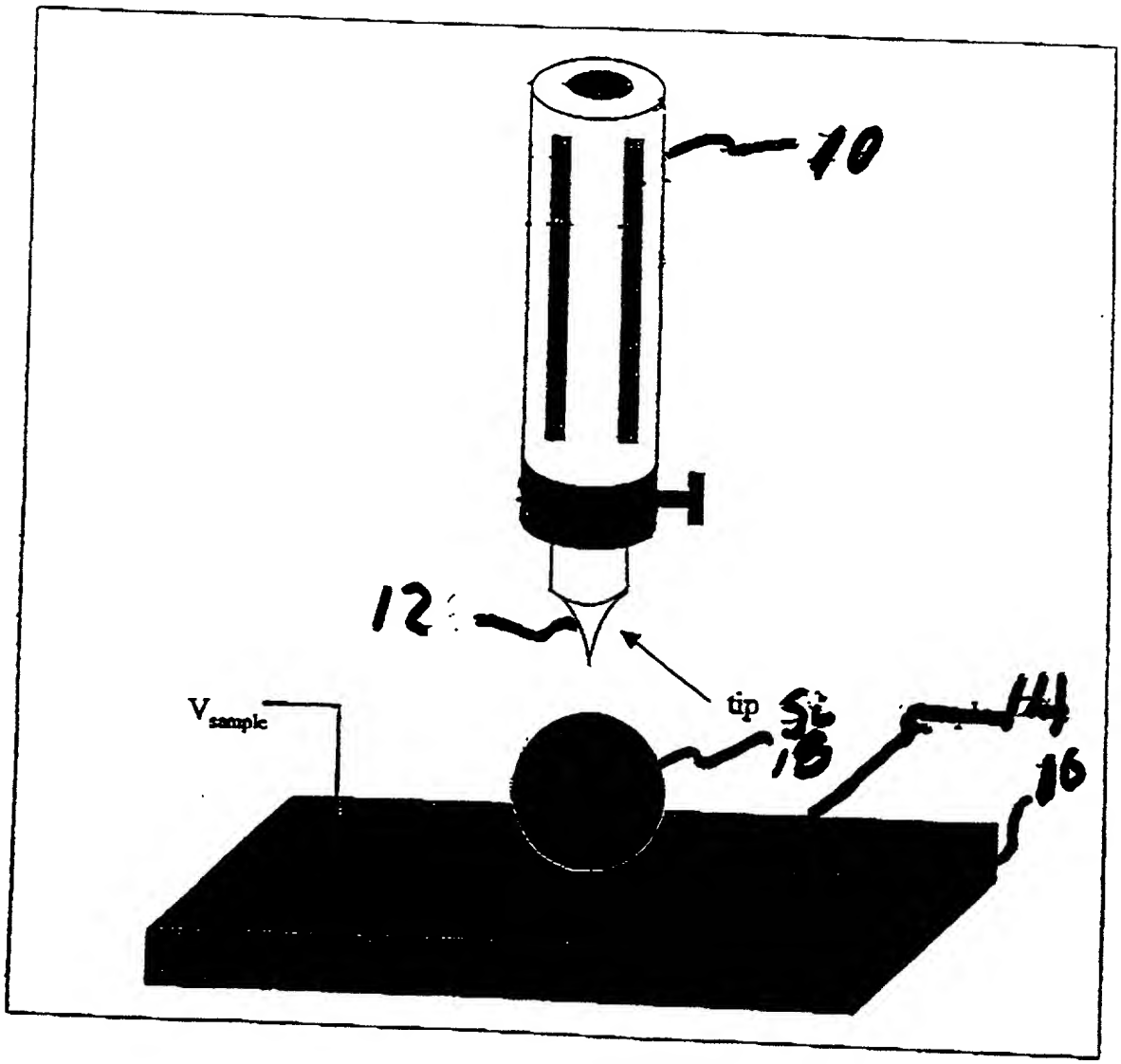


FIG 1

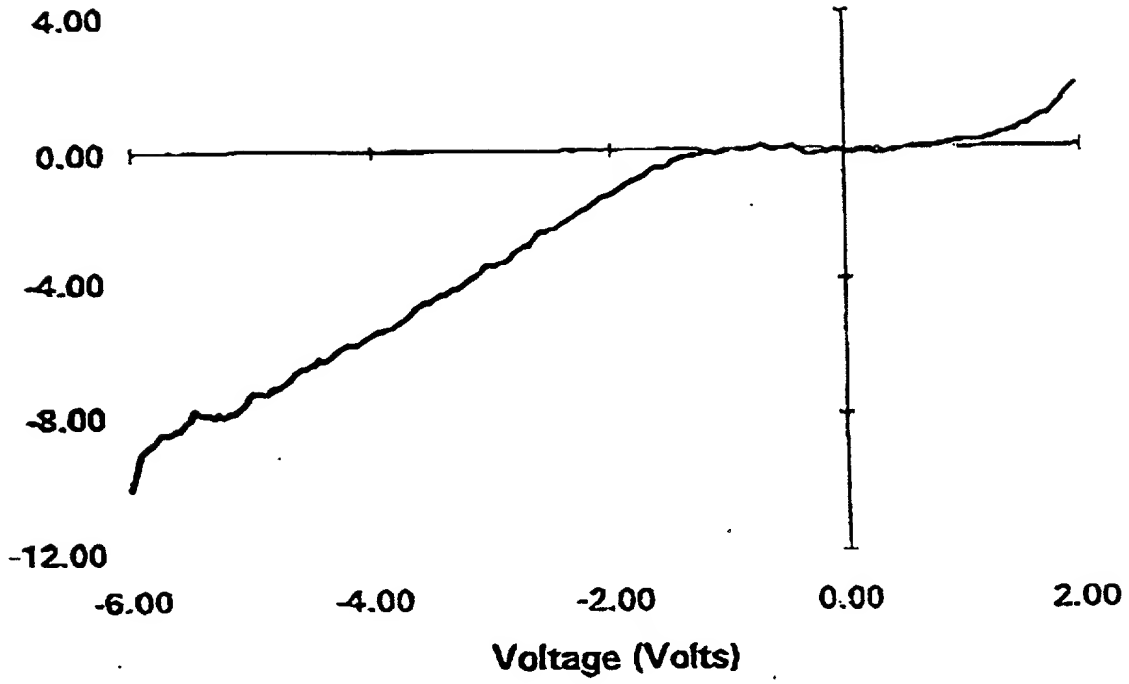

4.00
0.00
-4.00
-8.00
-12.00
Current (nA)
-6.00
-4.00
-2.00
0.00
2.00
Voltage (Volts)

FIG. 2

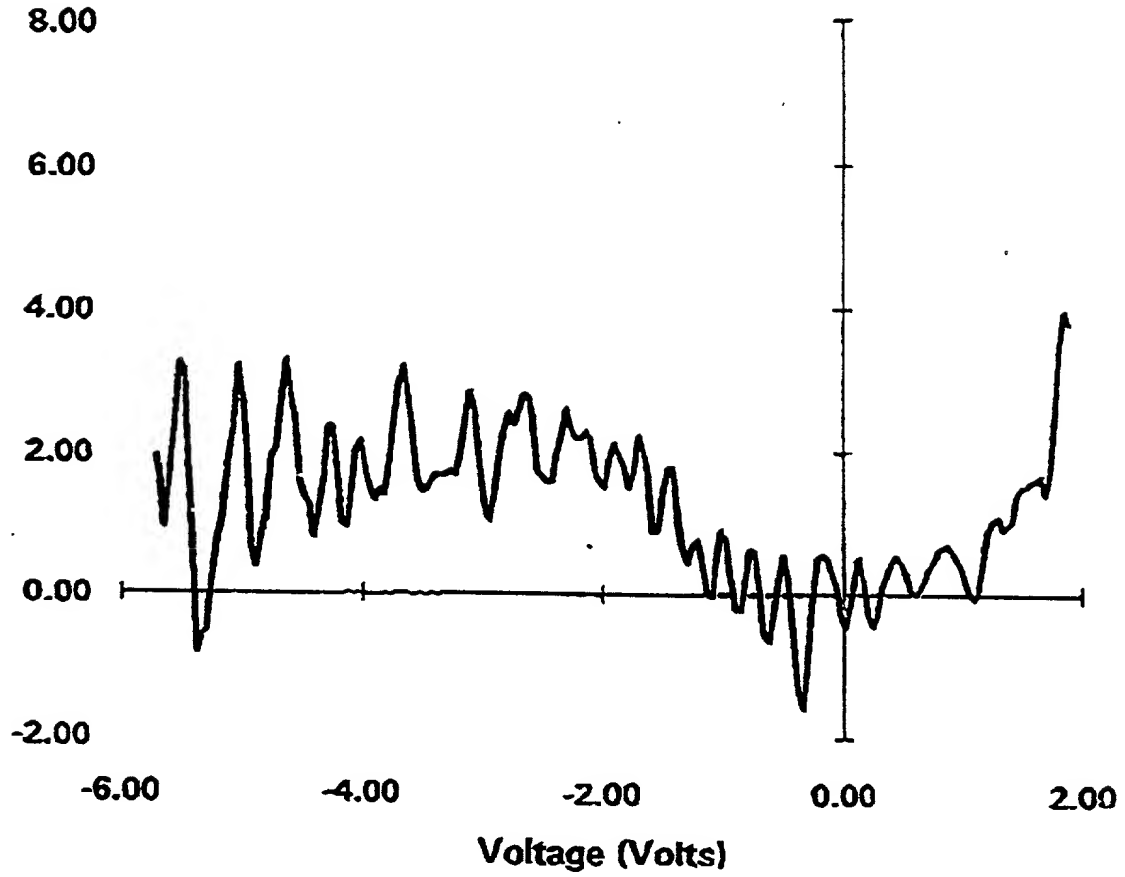

8.00
6.00
4.00
2.00
0.00
-2.00
dI/dV (nA/mV)
-6.00
-4.00
-2.00
0.00
2.00
Voltage (Volts)

FIG. 3

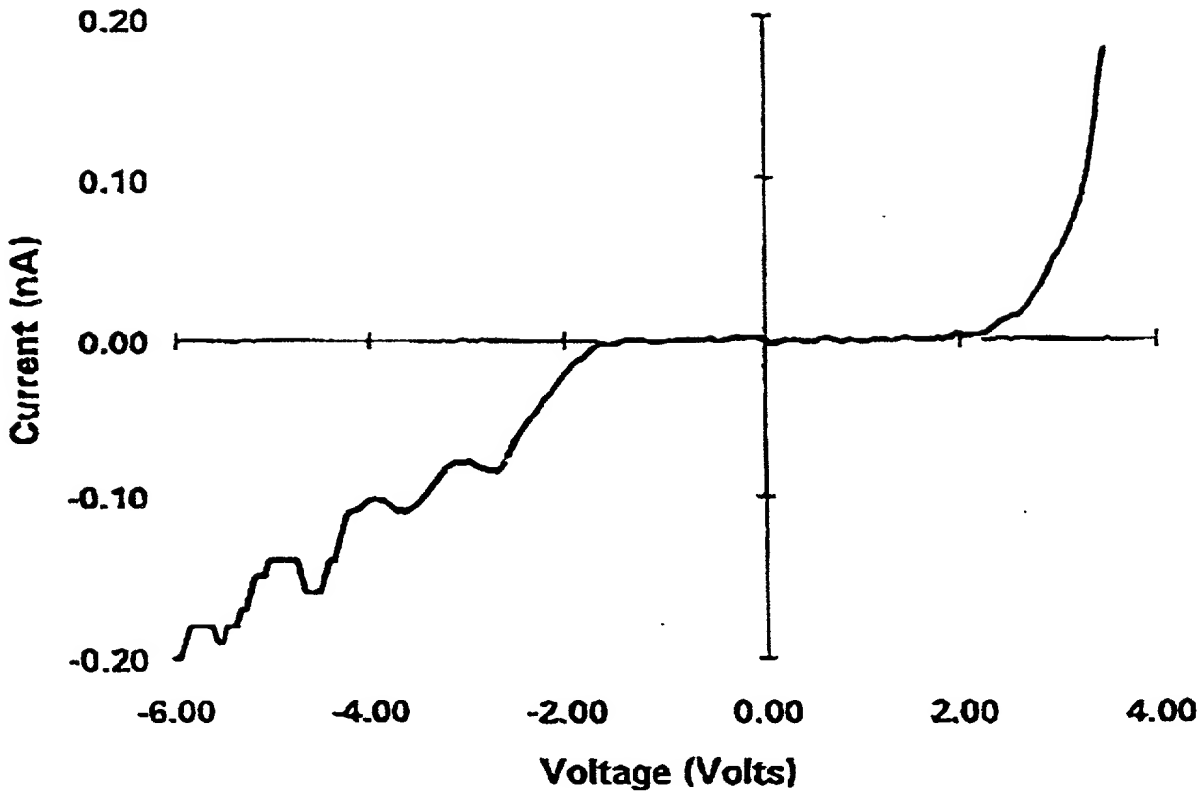

0.20
0.10
0.00
-0.10
-0.20
Current (nA)
-6.00
-4.00
-2.00
0.00
2.00
4.00
Voltage (Volts)

FIG. 4

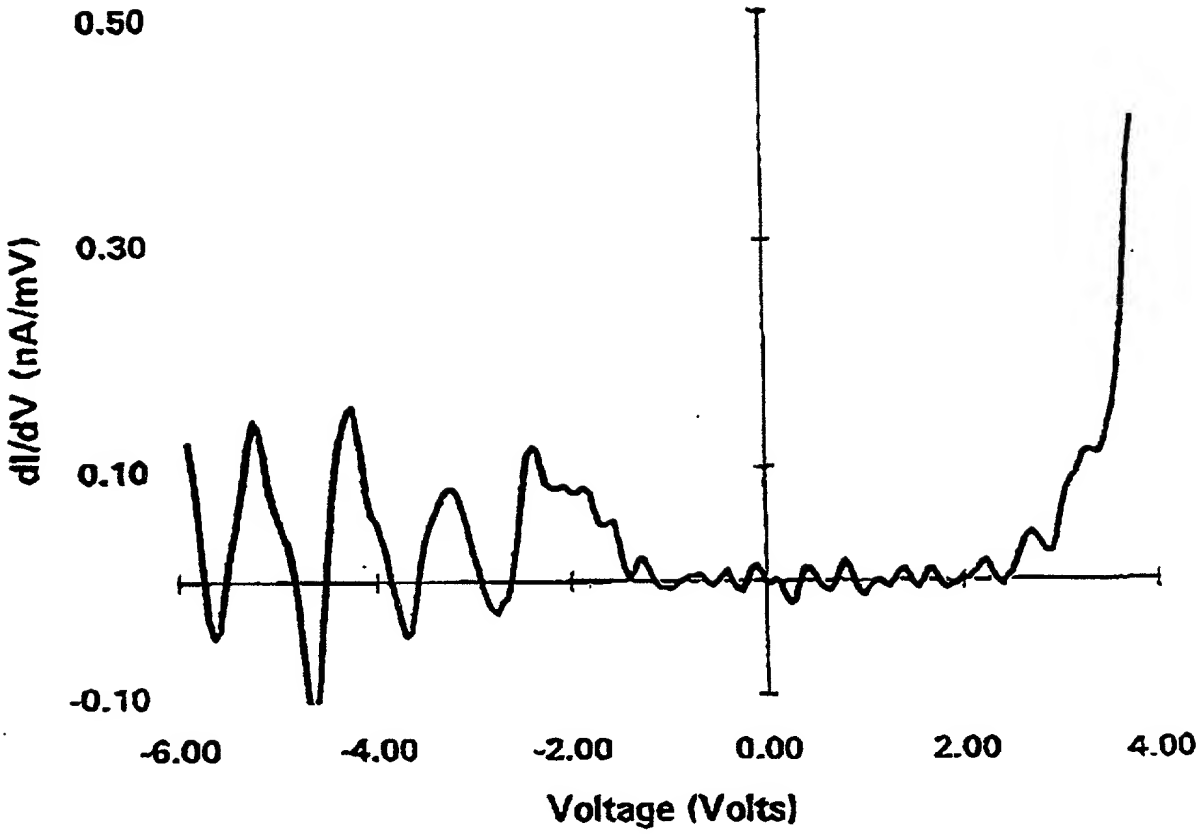

0.50
0.30
0.10
-0.10
dI/dV (nA/mV)
-6.00
-4.00
-2.00
0.00
2.00
4.00
Voltage (Volts)

FIG. 5

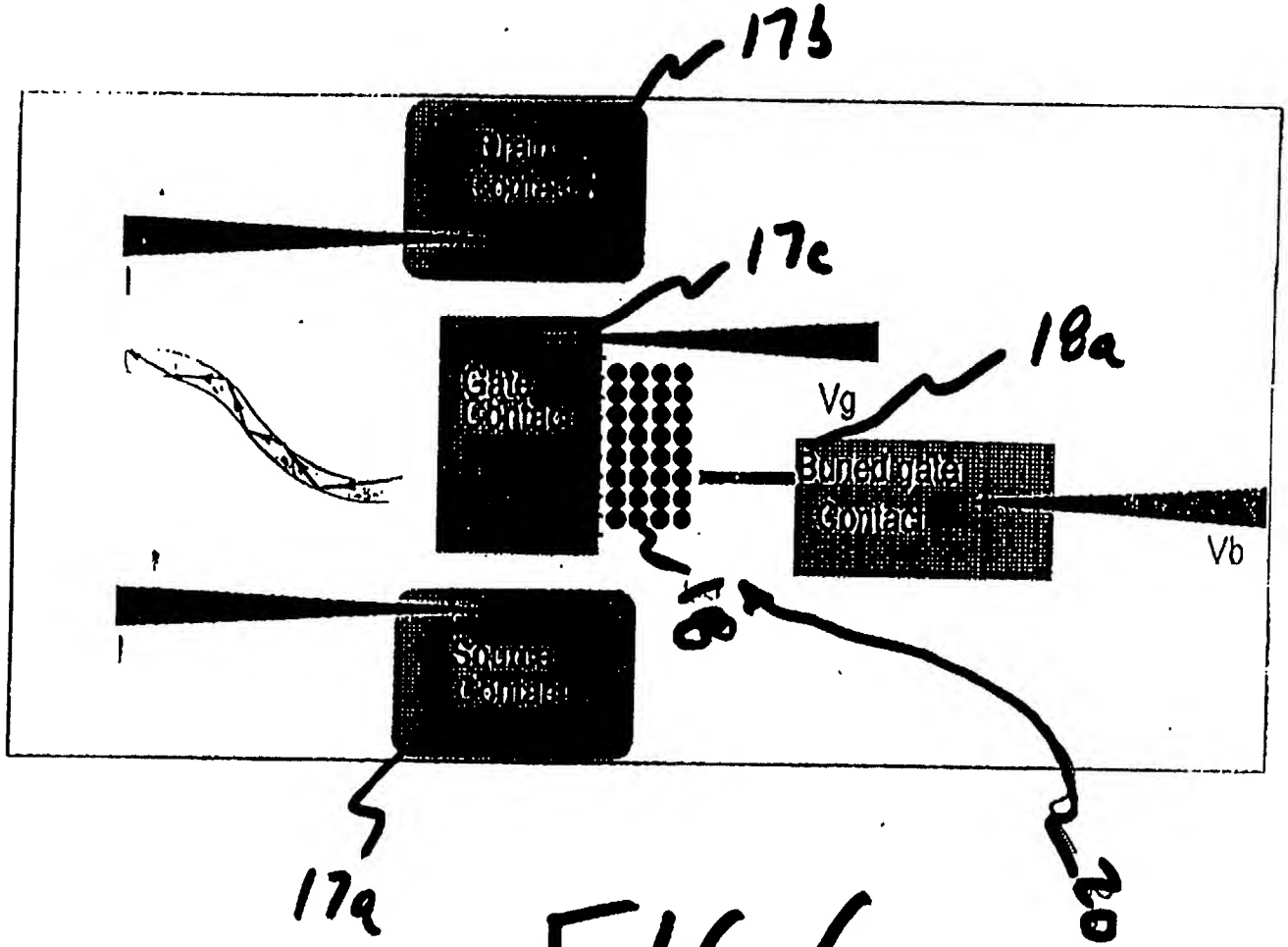


FIG 6

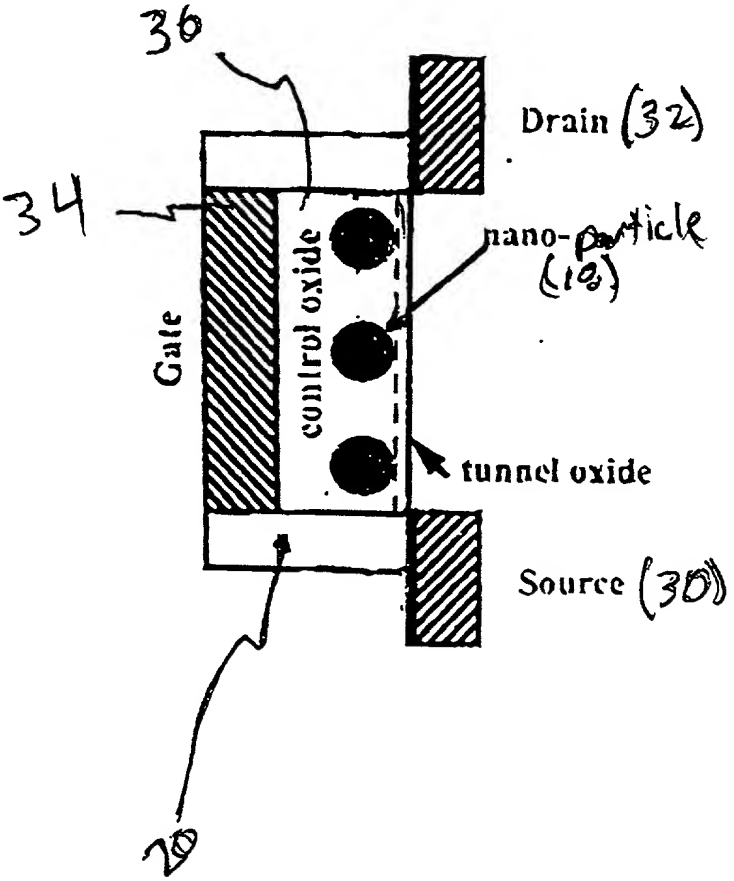
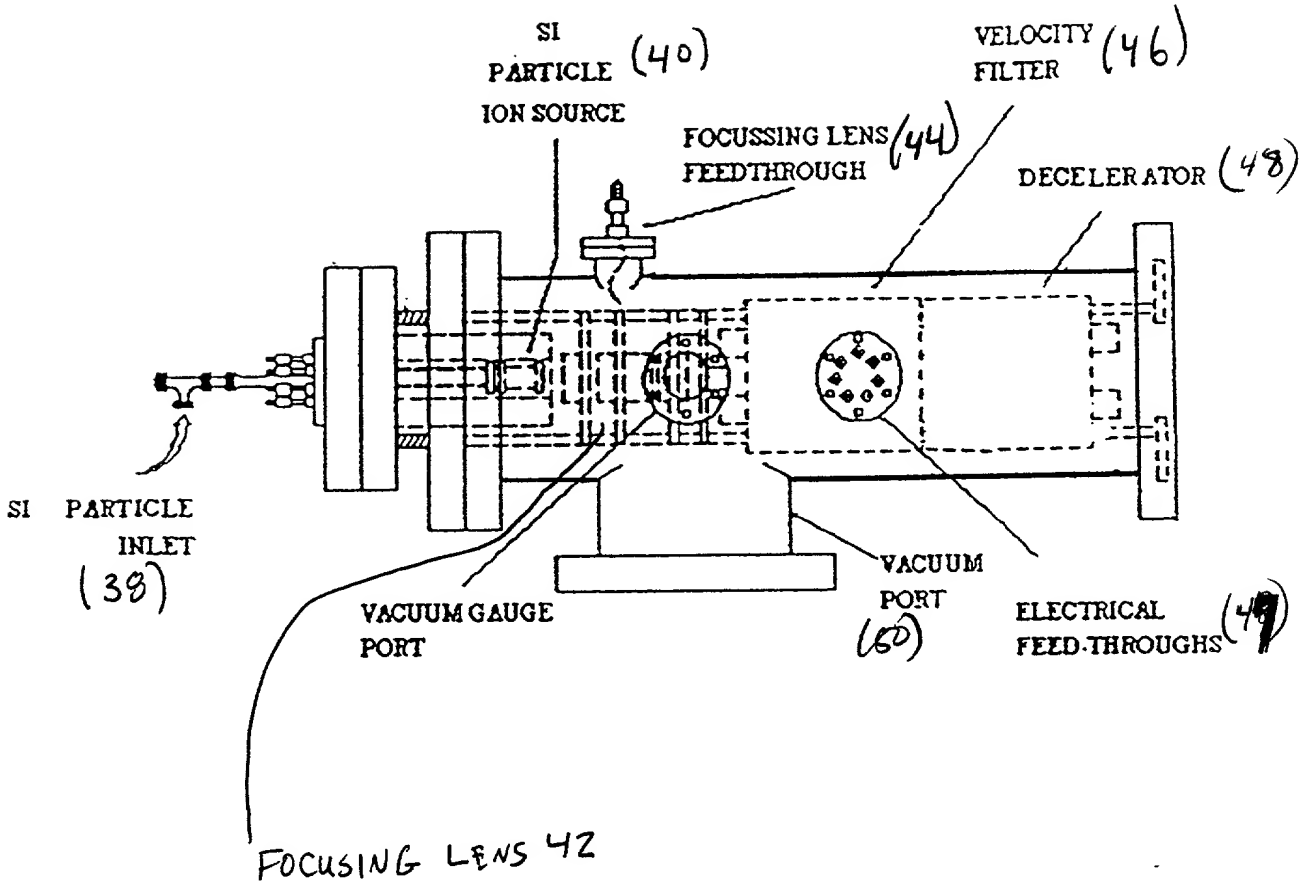

36
Drain (32)
34
nano-particle
(10)
Gate
control oxide
tunnel oxide
Source (30)
20

FIG. 1


SI PARTICLE ION SOURCE (40)
VELOCITY FILTER (46)
FOCUSSING LENS FEEDTHROUGH (44)
DECELERATOR (48)
SI PARTICLE INLET (38)
VACUUM GAUGE PORT
VACUUM PORT (60)
ELECTRICAL FEED-THROUGHS (49)
FOCUSING LENS 42

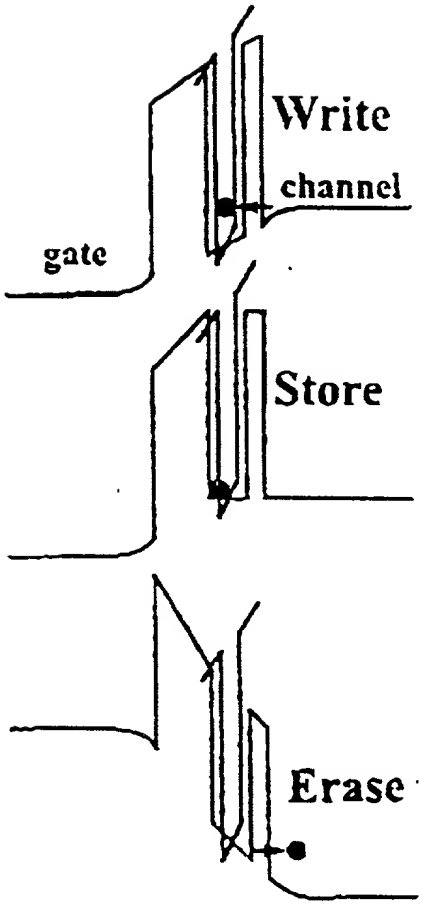


FIG. 9a

FIG. 9b

FIG. 9c

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare:

That my residence, post office address and citizenship are as stated below next to my name.

That I verily believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SILICON NANOPARTICLE FIELD EFFECT TRANSISTOR AND TRANSISTOR MEMORY DEVICE

the specification of which (check one)

(X) is attached hereto.

( ) was filed on _____ as
Application Serial No. _____
and was amended on _____
(if applicable)

That I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

That I acknowledge the duty to disclose information known to be material to patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

That I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

			Priority Claimed
_____	_____	_____	( ) Yes ( ) No
(Number)	(Country)	(Day/Month/Year Filed)	
_____	_____	_____	( ) Yes ( ) No
(Number)	(Country)	(Day/Month/Year Filed)	
_____	_____	_____	( ) Yes ( ) No
(Number)	(Country)	(Day/Month/Year Filed)	

That I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

United States Application(s)

09/426,204	10/25/99	Pending
(Application Serial No.)	(Filing Date)	(Status)-(Patented, pending, abandoned)
_____	_____	_____
(Application Serial No.)	(Filing Date)	(Status)-(Patented, pending, abandoned)
_____	_____	_____
(Application Serial No.)	(Filing Date)	(Status)-(Patented, pending, abandoned)

That all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

I hereby appoint the following attorneys and agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith and request that all correspondence and telephone calls in respect to this application be directed to GREER, BURNS & CRAIN, LTD., Suite 8660 - Sears Tower, 233 South Wacker Drive, Chicago, Illinois 60606, Telephone No. (312) 993-0080:

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Inventor's signature: _____

Date: _____

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_____

_____

Citizenship: _____

Full name of additional joint inventor, if any: _____

Inventor's signature: _____

Date: _____

Residence and Post Office Address: _____

_____

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Citizenship: _____

Full name of additional joint inventor, if any: _____

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